A 3V, 0.35μm CMOS Bluetooth Receiver IC

Wenjun Sheng, Bo Xia, Ahmed Emira, Chunyu Xin, Ari Yakov Valero-Lopez, Sung Tae Moon, Edgar Sánchez-Sinencio

Analog & Mixed Signal Center, Department of Electrical Engineering, Texas A&M University, College Station, TX 77843

Abstract **— This paper presents a monolithic low-IF Bluetooth receiver. The highlights of the receiver include a low-power active complex filter with a non-conventional tuning scheme and a high performance mixed-mode GFSK demodulator. The chip was fabricated on a 6.25 mm² die using TSMC 0.35μm standard CMOS process. –82 dBm sensitivity at 1e-3 BER, –10 dBm IIP3 and 15 dB noise figure were achieved in the measurements.**

I. Introduction

Bluetooth is a technology recently proposed enabling short range radio links between portable electronic devices [1]. Low cost, low power consumption and compactness are vital requirements for a Bluetooth transceiver due to its application environment. Several Bluetooth transceivers from industry have been recently reported [2]-[6]. Here, we introduce a fully integrated CMOS Bluetooth receiver designed in a university. The receiver is fabricated using a low cost 0.35μm standard CMOS process provided by MOSIS. The receiver uses a low-IF architecture with 2 MHz intermediate frequency (IF). A low power mixed mode GFSK demodulator that has a performance close to a digital optimum detector ensures a high sensitivity for the receiver. An on-chip automatically tuned OTA-C complex filter achieves more than 45dB image rejection ratio (IRR) and rejects strong adjacent channel interference.

II. System Design Considerations

In order to achieve a low power, low cost implementation, receiver architectures with a higher integration level, the *direct-conversion* and *low-IF* receivers, are the preferred topologies. Since a GFSK spectrum has significant energy at or near DC, the flicker noise and DC offset may significantly degrade the receiver performance in a direct-conversion receiver. On the other hand, a low-IF architecture with properly chosen IF may have relaxed image rejection requirement and negligible effect from flicker noise and DC offset. Thus, a *low-IF* architecture is selected in our design. Fig. 1 shows the block diagram of the proposed low-IF receiver. IF is chosen to be 2 MHz to provide a good compromise between the required IRR, the Q and power consumption of the complex filter. With 2 MHz IF, the required IRR is less than 35dB.

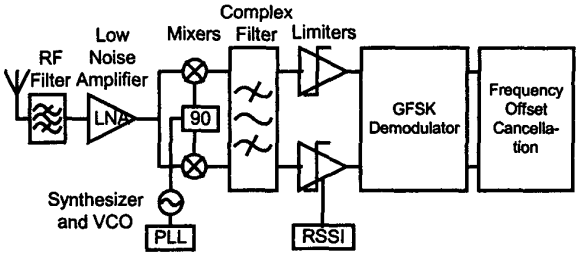


Fig. 1. Low-IF Bluetooth Receiver

III. Circuit Implementations

A fully differential topology is employed throughout the receiver circuits, among other things, to minimize the undesired coupling through low resistance substrate.

A. Low Noise Amplifier (LNA) and Mixer

A simplified schematic of the LNA and mixer is shown in Fig. 2. The LNA has a cascode topology with inductive source degeneration through an on-chip spiral inductor. The input matching network (Lg, Ls, M1) is designed considering the non-quasistatic effect. The performance of the LNA is optimized by properly choosing the size of the input and cascode transistors. The size of the input transistor M1 is chosen to obtain an effective Q of the amplifier input circuit for minimum noise figure (NF). The size of the cascode transistor M2 is chosen to be the same as M1 so that M1 and M2 can be laid out as a dual-gate transistor to minimize the parasitic capacitance at the drain of M1, thus improving the NF. The mixer is a modified double balanced Gilbert-Cell mixer. Extra current I_c is injected into the RF transistors to reduce the current flowing through the LO switches and load resistors, thus reducing the flicker noise contributed by the switches and allowing large load resistors which increase the conversion gain. Since the load of the mixer is resistive, the need of a common mode feedback (CMFB) circuit is avoided. The LNA and mixer have been tested as a single block, they consume 10mA current together from a 3V power supply. The measured cascaded NF and voltage gain are 8.5dB and 25dB, respectively. The cascaded IIP3 is around –9dBm.

0-7803-7246-8/02/$10.00 © 2002 IEEE

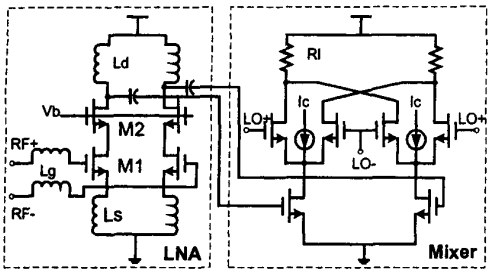


Fig. 2. Simplified LNA and Mixer schematic

B. *Active Complex Filter*

A complex bandpass filter (BPF) is obtained by applying a linear frequency transformation s->s-jω_c to a lowpass filter (LPF) prototype. This transformation is equivalent to replacing each pair of grounded capacitors by the circuit shown in Fig. 3(a) in an OTA-C filter [7]. Simulations show that a complex filter based on a 4th order Chebychev LPF or 6th order Butterworth LPF may be sufficient to achieve the required specifications. The Butterworth approximation is preferred for two reasons. First, it has smaller group delay variation. Second, all the poles will have the same angular frequency leading to better matching between the cross-coupled OTAs in the Butterworth filter. The highest Q in the LPF prototype is 2, which can be realized easily without using Q tuning. However, a frequency tuning circuit is required to compensate for large process variations. To simplify the LPF to BPF transformation, the LPF prototype has only grounded capacitors. The LPF prototype is implemented using three biquads. In order to reduce the input referred noise, the least number of transistors is used in the OTA (Fig. 3(b)). Long channel transistors (6 μm) are used to enhance the output resistance, improve matching, and reduce flicker noise. A pseudo differential architecture is used to reduce the required supply voltage. The common mode rejection ratio (CMRR) of the pseudo differential architecture is enhanced by using CMFB and common mode feed forward (CMFF) circuits. CMFB is used at high impedance nodes to enhance common mode (CM) stability while CMFF is used to isolate CM signals at different nodes. This efficient CM control helps to reduce noise and power, and increases the power supply rejection ratio (PSRR). Fig. 4 shows the I branch of the biquadratic section used in the filter. Note that the CM transconductance of the circuit shown in Fig. 3(b) is always negative. This means that a loop can be stable in differential mode (DM) but unstable in CM. OTA_1 and OTA_2 in Fig. 4 form a positive feedback loop in CM sense but a negative feedback loop in DM sense. A CMFF is used to break the CM loop by nulling OTA_2 CM transconductance. Since there is no resistor-connected OTA at node 2, a CMFB is used to stabilize this node. CMFF is also used in OTA_5 and OTA_6 to isolate the CM signals in I and Q branches, and in OTA_4 to isolate CM signals between biquads. This scheme uses only two CM detectors (CMDs), and hence it's more power and area efficient than using CMFB in each OTA. A CMRR in excess of 50dB is obtained. An automatic frequency tuning circuit using a relaxation oscillator is used to compensate for process variations. The complex filter consumes 4.7mA current. The measured IRR is more than 45dB.

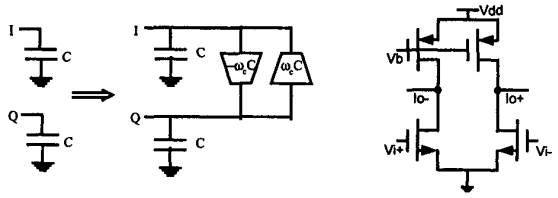


Fig. 3. (a) Linear frequency translation to convert LPF to complex BPF. (b) Pseudo differential OTA

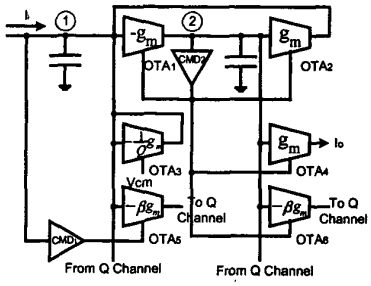


Fig. 4. I branch of the complex biquadratic section

C. *Frequency Synthesizer and VCO*

An integer-N frequency synthesizer generates the local oscillator signal. The frequency synthesizer has a reference frequency of 1MHz derived from a 16 MHz crystal oscillator. The divide by 15/16 dual modulus prescaler is followed by a level converter and programmable counters which are controlled from a serial interface. The prescaler is formed by a 3/4 divider and two divide-by-two flip flops. All the flip-flops in the prescaler are implemented using current mode logic. The fan out of the flip-flops in the 3/4 divider is smaller than that of more conventional architectures, increasing the speed of the prescaler. A third order on-chip passive loop filter is used. A buffer is inserted between the loop filter and the VCO to avoid the high frequency signal from the VCO leaking back to the loop filter, which will affect the operation of the synthesizer drastically. The VCO is a LC-tuned negative resistance oscillator. A 2-bit coarse tuning inversion mode varactor array is utilized to achieve a wide frequency tuning range to overcome the process variations while keeping the VCO gain low. A 2nd order polyphase network is used to generate quadrature outputs at 2.4GHz. This polyphase network is connected directly to the output of the VCO

without the need of an intermediate buffer, reducing the power consumption of the system. The schematic of the VCO is shown in Fig. 5. The tail current source of the VCO is connected to VDD instead of GND to improve the PSRR. The measured tuning range covers 350MHz with a VCO gain of 75MHz/V.

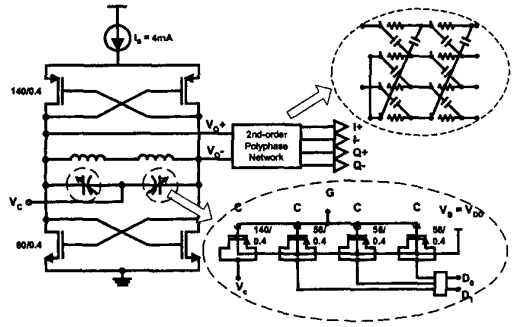


Fig. 5. VCO with varactor array

D. Limiter and GFSK Demodulator

The employed limiter architecture is a cascaded structure of five voltage gain cells (Fig. 6). Each cell provides 14dB gain, which makes the overall gain 70dB. A feedback type offset cancellation mechanism is employed to reduce the input offset voltage. A 26dB Received Signal Strength Indicator (RSSI) is an integral part of the limiting amplifier. The signals at the output of each amplifying cell are rectified by multiplier type rectifiers and summed up by resistors to provide a logarithmic output voltage. The I and Q outputs of the limiter feed a GFSK demodulator. The proposed demodulator is based on the zero-crossing detector (Fig. 7). Two zero-crossing detection (ZD) one-shots detect the positive and negative zero crossing points of input I and Q signals, and generate a narrow pulse (10ns) at each zero crossing moment. After the ZD one-shots, the pulses from both I and Q branches are combined together through OR gates and NOR gates. Another shape keeping (SK) one-shot is used to cancel the pulse width variation caused by process variations and mismatches between ZD one-shots. The SK one-shot generates a new train of equal width pulses. For the SK one-shot to work properly, its pulse width should be larger than the pulse width of any ZD one shot. The pulse width of SK one-shot is chosen to be 40ns, which is larger than any of ZD one shot pulse width even with large process variations. Thus, the demodulator is robust to process variations and mismatches. With a 40ns pulse width, some overlapping between pulses generated from I and Q channels may happen, and cause about 0.2dB performance degradation. Using both I and Q branches, instead of a single branch, improves performance by about 2dB. Since the active complex filter before the demodulator inherently has I and Q outputs, the extra silicon area and power consumption required are moderate. The measured demodulator performance shows a 16.2dB input SNR for 1e-3 BER, and 11.2dB co-channel interference performance. The demodulator consumes less than 3mA current.

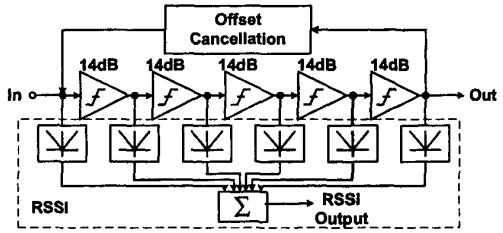


Fig. 6. Limiter and RSSI

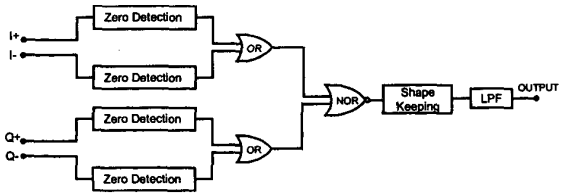


Fig. 7. GFSK Demodulator

E. Frequency Offset Cancellation Circuit

Bluetooth standard allows a frequency error in the center frequency of a transmitted signal as large as ±100 kHz in one time slot, including ±25 kHz frequency drifting [1]. This varying frequency offset needs to be cancelled to ensure the receiver performance. The frequency offset is translated to a DC offset voltage at the demodulator output. By integrating the 4 bits DC free preamble and trailer in the access code, we can get an estimation of the existing DC offset and subtract it from the demodulated signal. The frequency offset cancellation circuit following the demodulator is designed to fulfill two major tasks: detecting and canceling the offset during the access code transmission period, and tracking the variation of the frequency offset during the data transmission and re-correct it when it exceeds a certain threshold. The DC offset cancellation circuit works as an integrator during the reception of the access code, and as a very-low pass filter (20 kHz 3dB BW) during the data packets transmission, to track the frequency drifting. The total current consumption of the offset cancellation circuit is less than 1mA. The circuit can handle frequency errors up to ±150 kHz.

IV. Experimental Results

The receiver IC is fabricated in TSMC 0.35μm standard CMOS process, and packaged in a 48-pin TQFP plastic package. It takes 6.25 mm^2 silicon area. The die microphotograph is shown in Fig. 8. The receiver active

current is about 65 mA from a 3V power supply. An unexpected low Q (~2) of the on-chip inductors used in the VCO was obtained during the measurements. The problem is caused by the inaccuracy of the available simulator for on-chip spiral inductors, and the fact that several process parameters needed for the simulations are not available. The low Q of on chip spiral inductors forces extra current consumption of VCO buffers during the measurements. For a Q greater than 5, as expected, the total receiver current consumption would be less than 45 mA. In Fig. 9(a), the measured input return loss of the receiver is less than –12 dB in the whole Bluetooth band. In Fig. 9(b) the measured phase noise at 1MHz, 2MHz and 3 MHz are –118 dBc/Hz, -125 dBc/Hz and –130 dBc/Hz, respectively. Fig. 10(a) shows the measured noise spectrum at the filter output, the NF of receiver is 15 dB. Fig. 10(b) shows the complex filter frequency response for the signal and image sides. The IRR is 45dB. The filter attenuates the first and second adjacent channels by 27 and 58dB, respectively. In Fig. 11(a) the measured IIP3 is –10 dBm. The measured receiver BER versus the input RF signal power is shown at Fig. 11(b). At a 1e-3 BER, the minimum detectable signal is –82 dBm.

V. CONCLUSIONS

The development of the proposed Bluetooth receiver started from scratch. All system and circuits were obtained within a period of 12 months. This is probably the first functional Bluetooth receiver IC designed independently in a university environment, using a low cost standard CMOS process and meeting specifications. The key performance measurements are –82 dBm sensitivity at 1e-3 BER, –10 dBm IIP3 and 15 dB noise figure.

ACKNOWLEDGEMENTS

The authors are in debt to the RF IC Design Group from Texas Instruments and Wireless Subscriber Systems Group from Motorola for system and circuit design discussions. They also thank David Hernandez-Garduno and Alberto Valdes-Garcia for their assistance in the layout and PCB design and Shouli Yan for technical discussions.

REFERENCES

[1] Bluetooth Specification Version 1.0 B.

[2] A. Ajjkuttira, et.al., "A fully-integrated CMOS RFIC for Bluetooth applications," *IEEE International Solid-State Circuits Conference*, pp. 198 – 199, 2001.

[3] F.O. Eynde, et.al., "A fully-integrated single-chip SOC for Bluetooth," *IEEE International Solid-State Circuits Conference*, pp. 196 – 197, 2001.

[4] H. Darabi, et.al., "A 2.4 GHz CMOS Transceiver for Bluetooth," *IEEE International Solid-State Circuits Conference*, pp. 200 – 201, 2001.

[5] N. Filiol, et.al., "A 22mW Bluetooth RF transceiver with direct RF modulation and on-chip IF filtering," *IEEE International Solid-State Circuits Conference*, pp. 202 – 203, 2001.

[6] C. Durdodt, et.al., "The first very low-IF RX, 2-point modulation TX CMOS system on chip Bluetooth solution," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 99 – 102, 2001

[7] P. Andreani, S. Mattisson, and B. Essink, "A CMOS g_m-C polyphase filter with high image band rejection," 26th European Solid-State Circuits Conf., pp. 244–247, Sept. 2000.

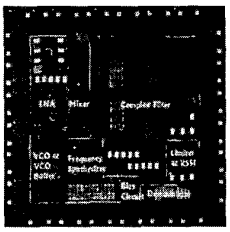
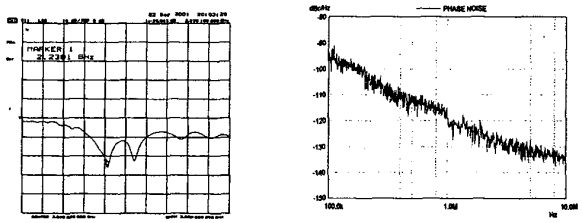
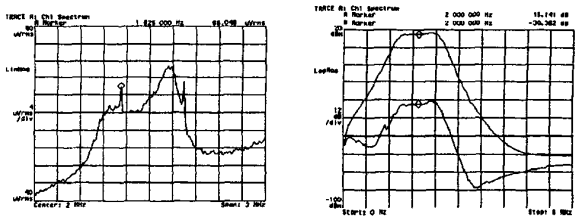


Fig. 8. Die microphotograph of Bluetooth receiver (6.25 mm^2)



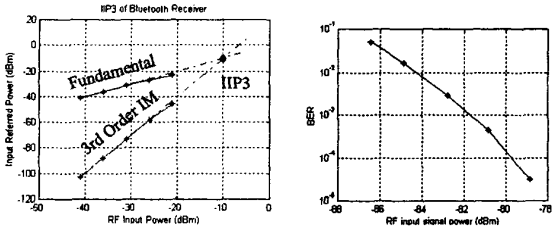
(a) (b)

Fig. 9. (a) Input return loss of receiver. (b) Phase noise



(a) (b)

Fig. 10. (a) Noise spectrum at complex filter output. (b) Complex filter frequency response for signal and image side



(a) (b)

Fig. 11. (a) IIP3 of receiver. (b) Measured BER vs. receiver input RF signal power